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MC68360

Product Brief

MC68360 QUad Integrated Communication Controller (QUICC™)

INTRODUCTION

The MC68360 QUad Integrated Communication Controller (QUICC™) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in communications activities. The QUICC (pronounced “quick”) can be described as a next-generation MC68302 with higher performance in all areas of device operation, increased flexibility, major extensions in capability, and higher integration. The term "quad" comes from the fact that there are four serial communications controllers (SCCs) on the device; however, there are actually seven serial channels: four SCCs, two serial management controllers (SMCs), and one serial peripheral interface (SPI).

QUICC Key Features

The following list summarizes the key MC68360 QUICC features:

- CPU32+ Processor (4.5 MIPS at 25 MHz)
  - 32-Bit Version of the CPU32 Core (Fully Compatible with the CPU32)
  - Background Debug Mode
  - Byte-Misaligned Addressing
- Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8 and 16 Bits)
- Up to 32 Address Lines (At Least 28 Always Available)
- Complete Static Design (0–25-MHz Operation)
- Slave Mode To Disable CPU32+ (Allows Use with External Processors)
  - Multiple QUICCs Can Share One System Bus (One Master)
  - MC68040 Companion Mode Allows QUICC To Be an MC68040 Companion Chip and Intelligent Peripheral (22 MIPS at 25 MHz)
  - Also Supports External MC68030-Type Bus Masters
  - All QUICC Features Usable in Slave Mode
- Memory Controller (Eight Banks)
  - Contains Complete Dynamic Random-Access Memory (DRAM) Controller
  - Each Bank Can Be a Chip Select or Support a DRAM Bank
  - Up to 15 Wait States
  - Glueless Interface to DRAM Single In-Line Memory Modules (SIMMs), Static Random-Access

Memory (SRAM), Electrically Programmable Read-Only Memory (EPROM), Flash EPROM, etc.
  - Four CAS lines, Four WE lines, One OE line
  - Boot Chip Select Available at Reset (Options for 8-, 16-, or 32-Bit Memory)
  - Special Features for MC68040 Including Burst Mode Support
- Four General-Purpose Timers
  - Superset of MC68302 Timers
  - Four 16-Bit Timers or Two 32-Bit Timers
  - Gate Mode Can Enable/Disable Counting
- Two Independent DMAs (IDMAs)
  - Single Address Mode for Fastest Transfers
  - Buffer Chaining and Auto Buffer Modes
  - Automatically Performs Efficient Packing
  - 32-Bit Internal and External Transfers
- System Integration Module (SIM60)
  - Bus Monitor
  - Double Bus Fault Monitor
  - Spurious Interrupt Monitor
  - Software Watchdog
  - Periodic Interrupt Timer
  - Low Power Stop Mode
  - Clock Synthesizer
  - Breakpoint Logic Provides On-Chip Hardware Breakpoints
  - External Masters May Use On-Chip Features Such As Chip Selects
  - On-Chip Bus Arbitration with No Overhead for Internal Masters
  - IEEE 1149.1 Test Access Port
- Interrupts
  - Seven External IRQ Lines
  - 12 Port Pins with Interrupt Capability
  - 16 Internal Interrupt Sources
  - Programmable Priority Between SCCs
  - Programmable Highest Priority Request
- Communications Processor Module (CPM)
  - RISC Controller
  - Many New Commands (e.g., Graceful Stop Transmit, Close RxBD)
  - 224 Buffer Descriptors
  - Supports Continuous Mode Transmission and Reception on All Serial Channels
  - 2.5 Kbytes of Dual-Port RAM
  - 14 Serial DMA (SDMA) Channels
  - Three Parallel I/O Registers with Open-Drain Capability
  - Each Serial Channel Can Have Its Own Pins (NMSI Mode)
- Four Baud Rate Generators
  - Independent (Can Be Connected to Any SCC or SMC)
  - Allows Changes During Operation
  - Autobaud Support Option

- Four SCCs
  - Ethernet/IEEE 802.3 Optional on SCC1 (Full 10-Mbps Support) (Available only on the MC68EN360)
  - HDLC/SDLC™ (All Four Channels Supported at 2 Mbps)
  - HDLC Bus (Implements an HDLC-Based Local Area Network (LAN))
  - AppleTalk®
  - Signaling System #7
  - Universal Asynchronous Receiver Transmitter (UART)
  - Synchronous UART
  - Binary Synchronous Communication (BISYNC)
  - Totally Transparent (Bit Streams)
  - Totally Transparent (Frame Based with Optional Cyclic Redundancy Check (CRC))
  - Profibus (RAM Microcode Option)
  - Asynchronous HDLC (RAM Microcode Option) to Support PPP (Point to Point Protocol)
  - DDCMP™ (RAM Microcode Option)
  - V.14 (RAM Microcode Option)
  - X.21 (RAM Microcode Option)
- Two SMCs
  - UART
  - Transparent
  - General Circuit Interface (GCI) Controller
  - Can Be Connected to the Time-Division Multiplexed (TDM) Channels
- One SPI
  - Superset of the MC68302 SCP
  - Supports Master and Slave Modes
  - Supports Multimaster Operation on the Same Bus
- Time-Slot Assigner
- Supports Two TDM Channels
  - Each TDM Channel Can Be T1, CEPT, PCM Highway, ISDN Basic Rate, ISDN Primary Rate, User Defined
  - 1- or 8-Bit Resolution
  - Allows Independent Transmit and Receive Routing, Frame Syncs, Clocking
  - Allows Dynamic Changes
  - Can Be internally Connected to Six Serial Channels (Four SCCs and Two SMCs)
- Parallel Interface Port
  - Centronics™ Interface Support
  - Supports Fast Connection Between QUICCs
- 240 Pins Defined: 241-Lead Pin Grid Array (PGA) and 240-Lead Plastic Quad Flat Pack (PQFP)

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™ DDCMP is a trademark of Digital Equipment Corporation.

™ Centronics is a trademark of Centronics, Inc.

QUICC ARCHITECTURE OVERVIEW

The QUICC is 32-bit controller that is an extension of other members of the Motorola M68300 family. Like other members of the M68300 family, the QUICC incorporates the intermodule bus (IMB). (The MC68302 is an exception, having an M68000 bus on chip.) The IMB provides a common interface for all modules of the M68300 family, which allows Motorola to develop new devices more quickly by using the library of existing modules. Although the IMB definition always included an option for an on-chip 32-bit bus, the QUICC is the first device to implement this option.

The QUICC is comprised of three modules: the CPU32+ core, the SIM60, and the CPM. Each module utilizes the 32-bit IMB. The MC68360 QUICC block diagram is shown in Figure 1.

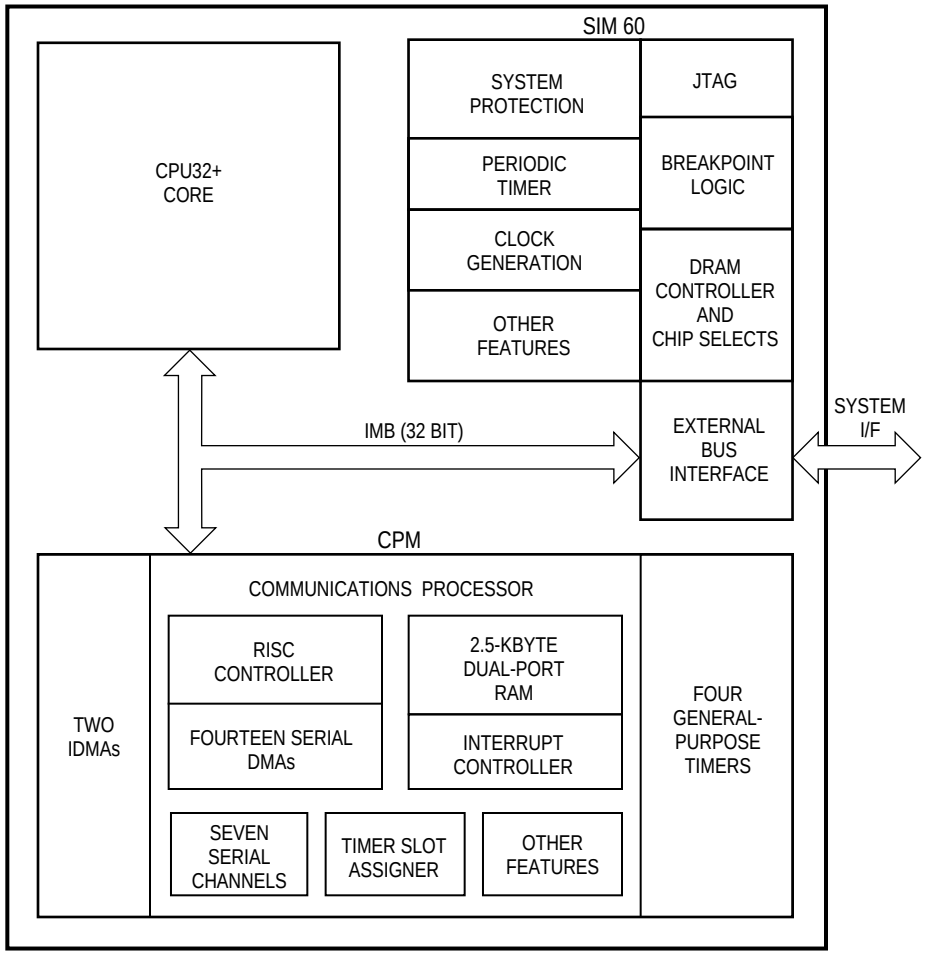


Figure 1. QUICC Block Diagram

CPU32+ Core

The CPU32+ core is a CPU32 that has been modified to connect directly to the 32-bit IMB and apply the larger bus width. Although the original CPU32 core had a 32-bit internal data path and 32-bit arithmetic hardware, its interface to the IMB was 16 bits. The CPU32+ core can operate on 32-bit external operands with one bus cycle. This allows the CPU32+ core to fetch a long-word instruction in one bus cycle and to

fetch two word-length instructions in one bus cycle, filling the internal instruction queue more quickly. The CPU32+ core can also read and write 32-bits of data in one bus cycle.

Although the CPU32+ instruction timings are improved, its instruction set is identical to that of the CPU32. It will also execute the entire M68000 instruction set. It contains the same background debug mode (BDM) features as the CPU32. No new compilers, assemblers, or other software support tools need be implemented for the CPU32+; standard CPU32 tools can be used.

The CPU32+ delivers approximately 4.5 MIPS at 25 MHz, based on the standard (accepted) assumption that a 10-MHz M68000 delivers 1 VAX MIPS. If an application requires more performance, the CPU32+ can be disabled, allowing the rest of the QUICC to operate as an intelligent peripheral to a faster processor. The QUICC provides a special mode called MC68040 companion mode to allow it to conveniently interface to members of the M68040 family. This two-chip solution provides a 22-MIPS performance at 25 MHz.

The CPU32+ also offers automatic byte alignment features that are not offered on the CPU32. These features allow 16 or 32-bit data to be read or written at an odd address. The CPU32+ automatically performs the number of bus cycles required.

System Integration Module (SIM60)

The SIM60 integrates general-purpose features that would be useful in almost any 32-bit processor system. The term “SIM60” is derived from the QUICC part number, MC68360. The SIM60 is an enhanced version of the SIM40 that exists on the MC68340 and MC68330 devices.

First, new features, such as a DRAM controller and breakpoint logic, have been added. Second, the SIM40 was modified to support a 32-bit IMB as well as a 32-bit external system bus. Third, new configurations, such as slave mode and internal accesses by an external master, are supported.

Although the QUICC is always a 32-bit device internally, it may be configured to operate with a 16-bit data bus. Regardless of the choice of the system bus size, dynamic bus sizing is supported. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode and 8- and 16-bit peripherals and memory to exist in the 16-bit system bus mode.

Communications Processor Module (CPM)

The CPM contains features that allow the QUICC to excel in communications and control applications. These features may be divided into three sub-groups:

- Communications Processor (CP)
- Two IDMA Controllers
- Four General-Purpose Timers

The CP provides the communication features of the QUICC. Included are a RISC processor, four SCCs, two SMCs, one SPI, 2.5 Kbytes of dual-port RAM, an interrupt controller, a time slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and fourteen serial DMA channels to support the SCCs, SMCs, and SPI.

The IDMAs provide two channels of general-purpose DMA capability. They offer high- speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The RISC controller may access the IDMA registers directly in the buffer chaining modes. The QUICC IDMAs are similar to, yet enhancements of, the two DMA channels found on the MC68340 and the one IDMA channel found on the MC68302.

The four general-purpose timers on the QUICC are functionally similar to the two general-purpose timers found on the MC68302. However, they offer some minor enhancements, such as the internal cascading of two timers to form a 32-bit timer. The QUICC also contains a periodic interval timer in the SIM60, bringing the total to five on-chip timers.

Upgrading Designs from the MC68302

Since the QUICC is a next-generation MC68302, many designers currently using the MC68302 may wish to use the QUICC in a follow-on design. The following paragraphs briefly discuss this endeavor in terms of architectural approach, hardware issues, and software issues.

Architectural Approach

The QUICC is the logical extension of the MC68302, but the overall architecture and philosophy of the MC68302 design remains intact in the QUICC. The QUICC keeps the best features of the MC68302, while making the changes required to provide for the increased flexibility, integration, and performance requested by customers. Because the CPM is probably the most difficult module to learn, anyone who has used the MC68302 can easily become familiar with the QUICC since the CPM architectural approach remains intact.

The most significant architectural change made on the QUICC was the translation of the design into the standard M68300 family IMB architecture, resulting in a faster CPU and different system integration features.

Although the features of the SIM60 do not exactly correspond to those of the MC68302 SIM, they are very similar. The QUICC SIM60 combines the best MC68302 SIM features with the best MC68340 SIM features for improved performance.

Because of the similarity of the QUICC SIM60 and CPU to other members of the M68300 family, such as the MC68332 and the MC68340, previous users of these devices will be comfortable with these same features on the QUICC.

Hardware Compatibility Issues

The following list summarizes the hardware differences between the MC68302 and the QUICC:

- Pinout—The pinout is not the same. The QUICC has 240 pins; the MC68302 has 132 pins.
- Package—Both devices offer PGA and PQFP packages. However, the QUICC PQFP package has a 20-mil pitch; whereas, the MC68302 PQFP package has a 25-mil pitch.
- System Bus—The system bus signals now look like those of the MC68030 as opposed to those of the M68000. It is still possible to interface M68000 peripherals to the QUICC, utilizing the same techniques used to interface them to an MC68020 or MC68030.
- System Bus in Slave Mode—A number of QUICC pins take on new functionality in slave mode to support an external MC68EC040. On the MC68302, the pin names generally remained the same in slave mode.
- Peripheral Timing—The external timings of the peripherals (SCCs, timers, etc.) are very similar (if not identical) to corresponding peripherals on the MC68302.
- Pin Assignments—The assignment of peripheral functions to I/O pins is different in several ways. First, the QUICC contains more general-purpose parallel I/O pins than the MC68302. However, the QUICC

offers many more functions than even a 240-pin package would normally allow, resulting in more multifunctional pins than the MC68302.

Software Compatibility Issues

The following list summarizes the major software differences between the MC68302 and the QUICC:

- Since the CPU32+ is a superset of the M68000 instruction set, all previously written code will run. However, if such code is accessing the MC68302 peripherals, it will require some modification.
- The QUICC contains an 8-Kbyte block of memory as opposed to a 4-Kbyte block on the MC68302. The register addresses within that memory map are different.
- The code used to initialize the system integration features of the MC68302 has to be modified to write the corresponding features on the QUICC SIM60. Code written for the MC68340 may be adapted in large part.
- As much as possible, QUICC CPM features were made identical to those of the MC68302 CP. The most important benefit is that the code flow (if not the code itself) will port easily from the MC68302 to the QUICC. The nuances learned from the MC68302 will still be useful in the QUICC.
- Although the registers used to initialize the QUICC CPM are new (for example, the SCM on the MC68302 is replaced with the GSMR and PSMR on the QUICC), most registers retain their original purpose such as the SCC event, SCC mask, SCC status, and command registers. The parameter RAM of the SCCs is very similar, and most parameter RAM register names and usage are retained. More importantly, the basic structure of a buffer descriptor (BD) on the QUICC is identical to that of the MC68302, except for a few new bit functions that were added. (In a few cases, a bit in a BD status word had to be shifted.)
- When porting code from the MC68302 CP to the QUICC CPM, the software writer may find that the QUICC has new options to simplify what used to be a more code-intensive process. For specific examples, see the INIT TX AND RX PARAMETERS, GRACEFUL STOP TRANSMIT, and CLOSE BD commands.

QUICC GLUELESS SYSTEM DESIGN

A fundamental design goal of the QUICC was ease of interface to other system components. An example of this goal is a minimal QUICC design using EPROM and DRAM, shown in Figure 2. This system interfaces gluelessly to an EPROM and a DRAM SIMM module. It also offers parity support for the DRAM.

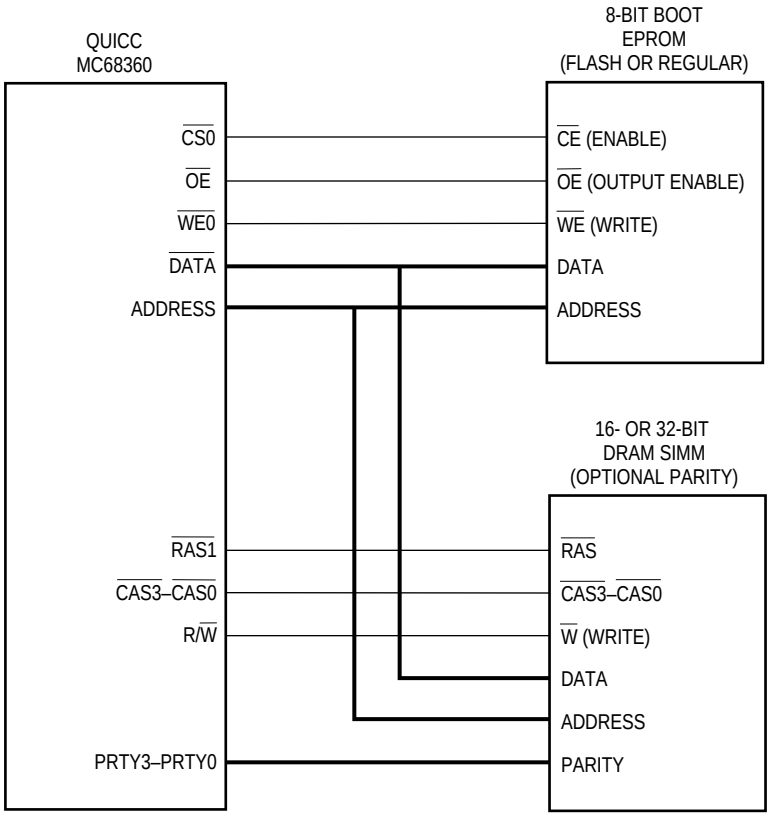


Figure 2. Minimum QUICC System Configuration

Figure 3 shows a larger system configuration. This system offers one EPROM, one flash EPROM, and supports two DRAM SIMMs. Depending on the capacitance on the system bus, external buffers may be required. From a logic standpoint, however, a glueless system is maintained.

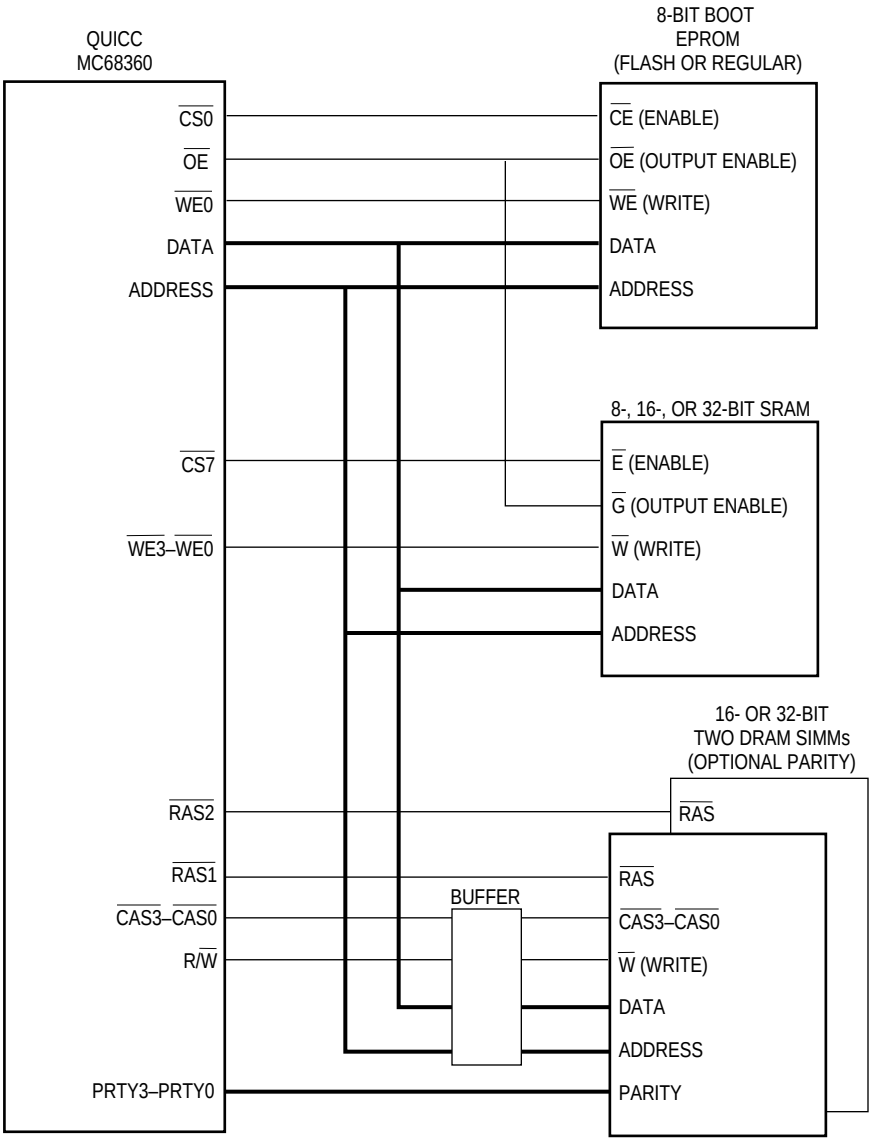


Figure 3. Larger QUICC System Configuration

QUICC Serial Configurations

The QUICC offers an extremely flexible set of communications capabilities. Although a full understanding of the possibilities requires reading the appropriate sections, some of the possibilities are shown in the following diagrams. They show possible connections between QUICC devices. In addition, connections are often shown between QUICCs and the MC68302 to show the compatibility between these devices.

For readability, transceivers are usually omitted in the following diagrams. For local on-board communications, however, transceivers are often optional and depend on the protocol used.

Figure 4 shows the Ethernet LAN capability of the QUICC. An external SIA transceiver is required to complete the interface to the media. This functionality is implemented in the MC68160 enhanced Ethernet serial transceiver (EEST™). The MC68160 EEST supports connections to the attachment unit interface (AUI) or twisted-pair Ethernet formats and provides a glueless interface to the QUICC.

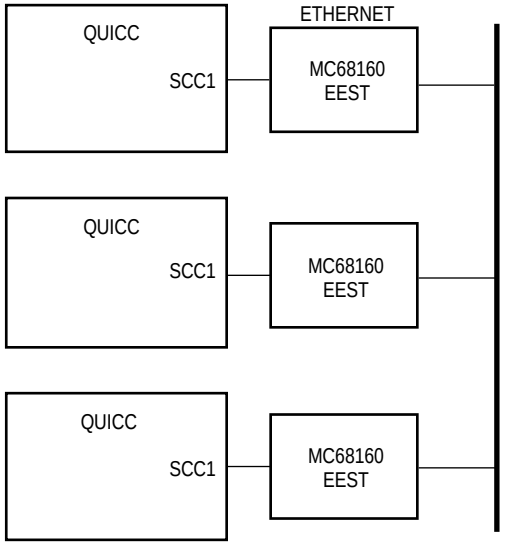
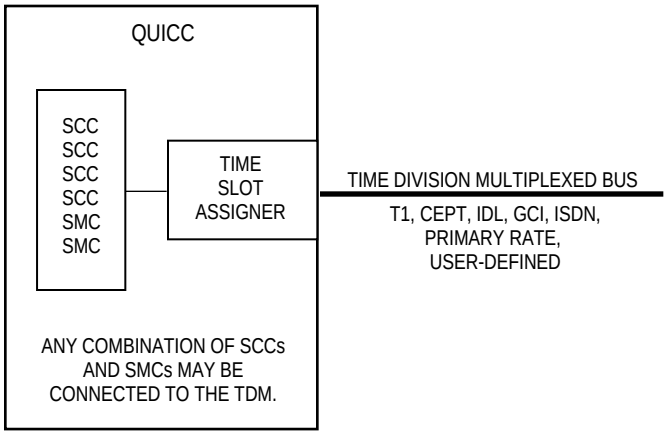


Figure 4. Ethernet LAN Capability

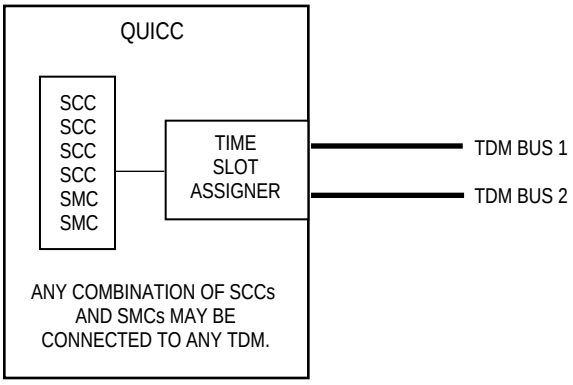
Figure 5 shows how up to six of the serial channels can connect to a TDM interface. The QUICC provides a built-in time-slot assigner for access to the TDM time slots. Other channels can work with their own set of pins, allowing possibilities like an Ethernet to T1 bridge, etc.



NOTE: Independent receive and transmit clocking, routing, and syncs are supported.

Figure 5. Serial Channel to TDM Bus Implementation

Figure 6 shows that the QUICC time-slot assigner can support two TDM buses. Each TDM bus can be of a different format—for example, one TDM can be a T1 line, and one can be a CEPT line. Also this technique could be used to bridge frames from basic rate ISDN to a T1/CEPT line, etc.



NOTE: Two TDM buses may be simultaneously supported with the time slot assigner.

Figure 6. Dual TDM Bus Implementation

QUICC Serial Configuration Examples

Figure 7 shows a general-purpose application that includes Ethernet, AppleTalk, an HDLC connection to a T1 line, an HDLC connection to frame relay, a UART debug monitor port, a totally transparent data stream port, and an SPI connection to a serial EEPROM.

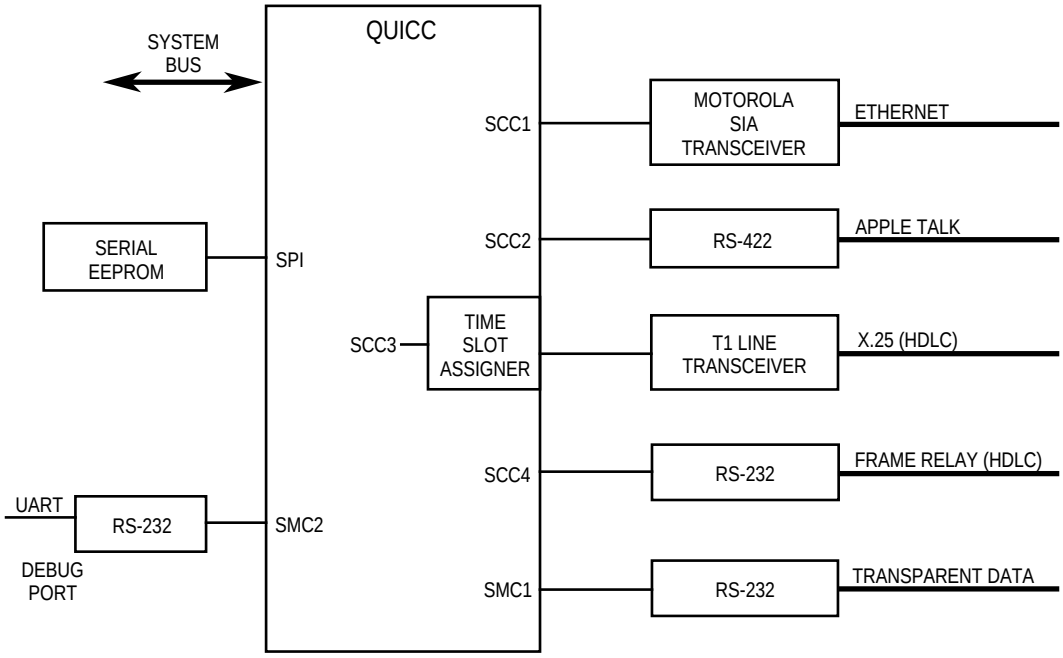


Figure 7. General-Purpose Application

QUICC System Bus Configurations

Figure 8 shows a master-slave QUICC configuration. This system gives eight SCCs, four SMCs, two SPIs, four IDMAs, etc. Each QUICC uses its own DMA capability, but the CPU32+ is the only processor in the system. More QUICCs can be easily supported on the system bus, if desired.

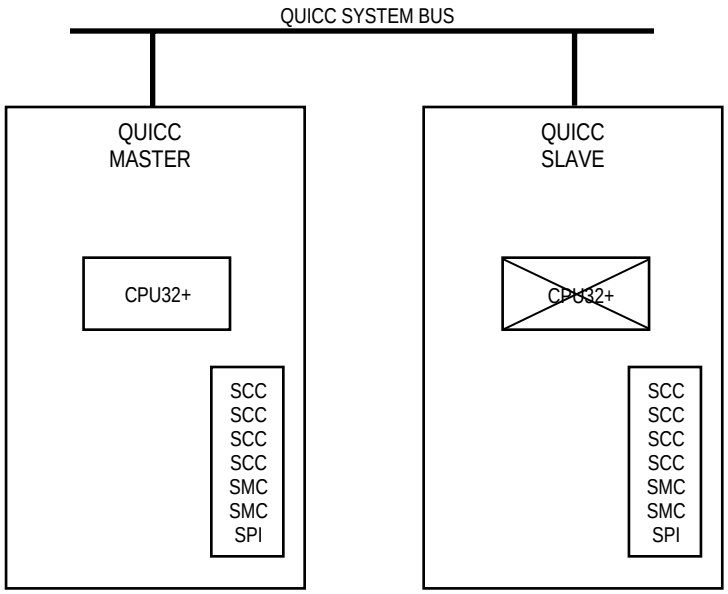


Figure 8. Master-Slave QUICC Implementation

The QUICC has special features in slave mode to support the M68040 family. When the QUICC is used in this way, it is said to be in MC68040 companion mode. Figure 9 shows how a QUICC in slave mode can interface to a MC68EC040. (The MC68EC040 is a low-cost version of the MC68040 with identical integer performance, but without the memory management unit (MMU) and the floating-point unit (FPU).) The DRAM controller on the QUICC will control the accesses of the MC68EC040 (including the burst modes). This configuration does require external address mutiplexers, but the QUICC controls the multiplexers. The QUICC supports the MC68EC040 in other ways, such as interrupt handling and system protection features. When it is in slave mode, the QUICC can also be interfaced to any MC68030-type bus master instead of the MC68EC040.

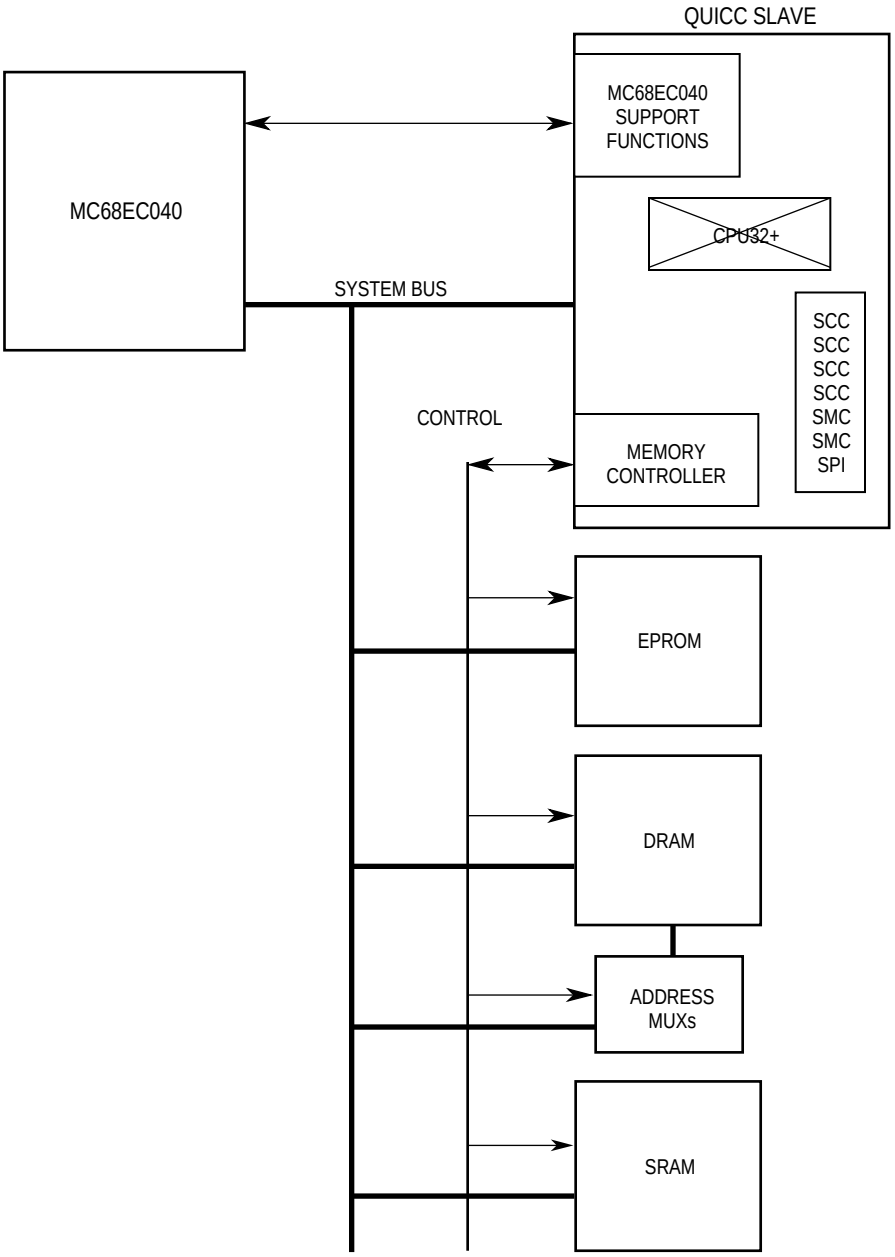


Figure 9. MC68040 Companion Mode

The following table identifies the packages and operating frequencies available for the MC68360.

MC68360 Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature	Order Number
Quad Flat Pack (EM Suffix)	0–25	0°C to 70°C	MC68360EM25
Quad Flat Pack (EM Suffix)	0–25	–40°C to +85°C	TBD
Quad Flat Pack with Ethernet	0–25	0°C to 70°C	MC68EN360EM25
Quad Flat Pack with Ethernet	0–25	–40°C to +85°C	TBD
Pin Grid Array (RC Suffix)	0–25	0°C to 70°C	MC68360RC25
Pin Grid Array (RC Suffix)	0–25	–40°C to +85°C	TBD
Pin Grid Array with Ethernet	0–25	0°C to 70°C	MC68EN360RC25
Pin Grid Array with Ethernet	0–25	–40°C to +85°C	TBD

The documents listed in the following table contain detailed information on the MC68360. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Documentation

Document Title	Order Number	Contents
MC68360 User's Manual	MC68360UM/AD	Detailed Information for Design
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set
The 68K Source	BR729/D	Independent Vendor Listing Supporting Software and Development Tools

Literature Distribution Centers:

USA: Motorola Literature Distribution: P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive Blakelands, Milton Keynes, MK14 5BP, England.
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ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.